

Amendments to the Claims

The listing of claims will replace all prior versions, and listings, of claims in the application:

5

Listing of Claims:

Claims 1-16 (Cancelled)

- 10 Claim 17 (Previously Presented): A clock generating circuit, comprising:
a clock generator for receiving a reference clock signal and thereby generating an
output clock signal; and
a spread spectrum control circuit, coupled to the clock generator, for generating a
modulated clock signal with frequency variation according to the output clock
15 signal and a modulation value, comprising:
a modulation value generating circuit for outputting the modulation value; and
a frequency control circuit, coupled to the clock generator and the modulation
value generating circuit, for generating the modulated clock signal according to
the output clock signal and the modulation value with which an average
20 frequency of the modulated clock signal varies;
wherein the clock generator operates in a way being independent of the spread
spectrum control circuit, and the modulation value varies with time in a
predetermined manner so as to force the average frequency of the modulated clock
signal to change up and down over time.

25

Claim 18 (Previously Presented): The clock generating circuit of claim 17, wherein the
predetermined manner represents that the modulation value increases progressively
in a first period of time and then decreases progressively in a second period of time

so as to force the average frequency of the modulated clock signal to change over time.

5 Claim 19 (Previously Presented): The clock generating circuit of claim 17, wherein the modulation value generating circuit outputs the modulation value according to at least one of an external control and the average frequency of the modulated clock signal.

10 Claim 20 (Previously Presented): The clock generating circuit of claim 17, wherein the spread spectrum control circuit further comprises:
a timing control circuit, coupled between the modulation value generating circuit and the frequency control circuit, for providing a frequency control value for the frequency control circuit according the modulation value after a predetermined period of time such that the average frequency of the modulated clock signal
15 changes in accordance with the frequency control value after the predetermined period of time.

20 Claim 21 (Previously Presented): The clock generating circuit of claim 20, wherein the timing control circuit is a delta-sigma modulator.

Claim 22 (Previously Presented): The clock generating circuit of claim 17, wherein the clock generator is a multi-phase clock generator for generating the output clock signal including a plurality of oscillation clock signals having a same frequency but different phases.

25 Claim 23 (Previously Presented): The clock generating circuit of claim 22, wherein the frequency control circuit comprises:
a phase interpolator, coupled to the clock generator, for generating a plurality of

interpolation signals according to at least two of the oscillation clock signals; and
a phase selector, coupled to the phase interpolator and the modulation value
generating circuit, for receiving the plurality of interpolation signals and
outputting one of them as the modulated clock signal according to the modulation
5 value.

Claim 24 (Previously Presented): The clock generating circuit of claim 22, wherein the
frequency control circuit comprises:
a phase selector, coupled to the clock generator, for outputting at least two of the
10 oscillation clock signals as selection signals; and
a phase interpolator, coupled to the phase selector, for generating the modulated
clock signal according to the selection signals;
wherein at least one of the phase selector and the phase interpolator operates
according to the modulation value.

15 Claim 25 (Previously Presented): A clock generating method, comprising:
generating an output clock signal according to a reference clock signal; and
executing a spread spectrum control step for generating a modulated clock signal
with frequency variation according to the output clock signal and a modulation
20 value, the spread spectrum control step comprising:
generating the modulation value; and
generating the modulated clock signal according to the output clock signal and the
modulation value with which an average frequency of the modulated clock
signal varies;
25 wherein the output clock signal is generated in a way being independent of the
spread spectrum control step, and the modulation value varies with time in a
predetermined manner so as to force the average frequency of the modulated clock
signal to change up and down over time.

Claim 26 (Previously Presented): The clock generating method of claim 25, wherein the predetermined manner represents that the modulation value increases progressively in a first period of time and then decreases progressively in a second period of time
5 so as to force the average frequency of the modulated clock signal to change over time.

Claim 27 (Previously Presented): The clock generating method of claim 25, wherein the step of generating the modulation value is executed according to at least one of an
10 external control and the average frequency of the modulated clock signal.

Claim 28 (Previously Presented): The clock generating method of claim 25, wherein the spread spectrum control step further comprises:
generating a frequency control value according the modulation value after a
15 predetermined period of time such that the average frequency of the modulated clock signal changes in accordance with the frequency control value after the predetermined period of time.

Claim 29 (Previously Presented): The clock generating method of claim 25, wherein the
20 output clock signal includes a plurality of oscillation clock signals having a same frequency but different phases.

Claim 30 (Previously Presented): The clock generating method of claim 29, wherein the step of generating the modulated clock signal comprises:
25 generating a plurality of interpolation signals according to at least two of the oscillation clock signals; and
receiving the plurality of interpolation signals and outputting one of them as the modulated clock signal according to the modulation value.

Claim 31 (Previously Presented): The clock generating method of claim 29, wherein the step of generating the modulated clock signal comprises:

receiving the oscillation clock signals and outputting at least two of them as

5 selection signals; and

generating the modulated clock signal according to the selection signals;

wherein at least one of the step of outputting the selection signals and the step of
generating the modulated clock signal according to the selection signals is
executed according to the modulation value.

10

Claims 32-39 (Cancelled)